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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
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10/725,938

12/03/2003

Holger Hoppe

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07/18/2006

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EXAMINER

NGUYEN, VINH P

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                        |                     |  |
|------------------------------|------------------------|---------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |  |
|                              | 10/725,938             | HOPPE, HOLGER       |  |
|                              | <b>Examiner</b>        | <b>Art Unit</b>     |  |
|                              | VINH P. NGUYEN         | 2829                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-17, 19-21, 23 and 24 is/are rejected.
- 7) ☒ Claim(s) 4, 18 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of “contacting test contacts” as recited in claims 1 and 12, “pad/pads of the semiconductor chip” and “pad/pads of the carrier” as recited in claims 8-9 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Claims 1-24 are objected to because of the following informalities:

In claim 1, it is unclear what “one or more contacting test contacts” comprises of. Are

they shown in any of drawings?

In claim 4, it is unclear what has been claimed since the limitation of this claim is not further limited the scope of the claim.

In claim 7, it is unclear how the testing time frame is determined less than 2 second after loading of the carrier with the semiconductor chip . Which device is used for determining this testing time frame.

In claim 8, it is unclear how the pad of the semiconductor chip is interrelated and associated with the contacting test contacts in claim 1.

In claim 13, it is unclear what “ a loading chip” comprises of.

In claims 16,18,20-22, it is unclear what “additional contact” comprises of. Is it shown in any of drawings?

The dependent claims not specifically address share the same indefiniteness as they depend from rejected base claims.

Appropriate correction is required.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3,5-17,19-21 and 23-24 are rejected under 35 U.S.C. 102( b) as being anticipated by Matsuda (Pat # 4,730,156).

As to claims 1 and 12-13, Matsuda discloses in figure # 2 an apparatus for testing contacting between a semiconductor chip and a carrier having a carrier (16a,16b,16c,16d) for coupling to a semiconductor chip (10a,10b,10c,10d) and a plurality of contacting test contacts (162a,162b,162c,162d) for exclusively testing the contacting between the semiconductor chip and the carrier (16a,16b,16c,16d).

As to claims 2 and 14, it appears that the carrier (162a,162b,162c,162d) electrically coupled to a testing apparatus (30,34,32,36).

As to claim 3, it appears that the carrier is connected to the testing apparatus and the carrier (16a,16b,16c,16d) is subsequently loaded with semiconductor chip (10a,10b,10c,10d).

As to claims 5 and 13, the contacting between the carrier and the chip is tested by the testing apparatus (30,34,32,36).

As to claim 6, the device of Matsuda is configured to test the contacting between the carrier and the semiconductor chip but not functioning of the chip.

As to claim 7, performing the contacting between the carrier and the semiconductor chip being tested by the testing apparatus (34,30,32,36) less than 2 seconds after loading of the carrier with the chip is considered as an inherent function of the testing apparatus (30,32,34 and 36).

As to claims 8-9, the contacting testing between the carrier and the chip is determined whether an electric contact has been established between a corresponding pad (104a,106a,104b,106b,104c,106c,104d,106d) and the assigned pads (162a,164a,162b,164b,162c,164c,162d,164d) of the carrier (16a,16b,16c,16d).

As to claim 10, it appears that there is a current flowing through the corresponding chip pad to the testing apparatus (30,34,32,36) in order to trigger the indicator (36) for indicating the electric contact between the chip and the carrier.

As to claim 11, when the contact between the semiconductor chip and the carrier is properly connected, the indicator (36) is lit up, that means there is an amount of voltage dropping across the chip pad and that voltage is determined by the indicator (36).

As to claims 15 and 19, it appears that some of the contacting test contacts (see figure 2 , test contacts on the upper left corner of the chip (10a,10b,10c,10d) are not used during ordinary operation of the chip.

As to claims 16 and 20, Matsuda also disclose additional contact (104 or 106).

As to claims 17 and 21, the contacts (104a, 106a,104b,106b,104c,106c,104d,106d) are not used for testing the functioning of the chip during contacting test between the semiconductor chip and the carrier.

As to claims 23-24, Matsuda discloses one or more contacting test contacts (104a,106a,104b,106b,104c,106c,104d,106d) are provided on a bottom of the chip (10a,10b,10c,10d).

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Parsons (Pat # 4,864,219) disclose method and apparatus for verifying proper placement of integrated circuits on circuit boards.

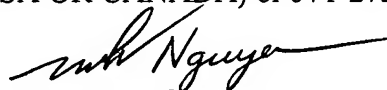
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964. The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, HA T. NGUYEN can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for

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unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
VINH P NGUYEN  
Primary Examiner  
Art Unit 2829  
07/17/06